REMARKS

Applicant appreciates the detailed examination evidenced by the Office Action mailed August 11, 2005 (hereinafter "Office Action"). Applicant has amended Claim 1 to correct a minor typographical error. Applicant has added new Claims 37 and 38, and respectfully traverses the rejections of Claims 1-18 for at least the reasons discussed below.

Independent Claims 1 and 13 are patentable

Independent Claims 1 and 13 stand rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,528,896 to Song et al. (hereinafter "Song"). Claim 1 recites:

> A memory device comprising:
> a semiconductor substrate;
> a first gate insulator on a first portion of a semiconductor substrate;
> a storage node on the first gate insulator;
> a tunnel junction barrier on the storage node;
> a data electrode on the tunnel junction barrier;
> a second gate insulator on a sidewall of the tunnel junction barrier;
> ***a third gate insulator*** on a second portion of the substrate adjacent the tunnel junction barrier;
> a gate electrode on the second gate insulator ***and the third gate insulator***; and
> first and second impurity-doped regions in the substrate coupled by ***a channel through the first and second portions of the substrate.***

FIGs. 2 and 3 illustrate examples of a device according to some embodiments of Claim 1. Referring to FIG. 3, the regions 103a, 105a, 110a and 120a provide "a first gate insulator," "a storage node," "a tunnel junction barrier" and "a data electrode," respectively. A vertical portion of the layer 130 along a sidewall of the region 110a provides "a second gate insulator." A horizontal portion of the layer 130 extending laterally adjacent the region 103a provides "a third gate insulator." The layer 132a, which has a vertical portion conforming the above-described vertical portion of the layer 130 and a horizontal portion conforming to the above-described horizontal portion of the layer 130, provides a gate electrode "on the second gate insulator and the third gate insulator." Regions 147, which, as shown in FIG. 2, are disposed on respective sides of the region 110a, provide "first and second impurity-doped regions." The regions are coupled via first and second channels 140, 145b "through the first and second portions of the substrate."

The Office Action cites FIG. 1(a) of Song as teaching "a semiconductor substrate," "a first gate insulator on a first portion of the semiconductor substrate," and a "storage node . . . on the first gate insulator." Office Action, p. 3. The Office Action cites FIG. 1(d) of Song as teaching "a tunnel junction barrier 4 on the storage node," "a data electrode . . . on the tunnel junction barrier," "a third gate insulator on a second portion of the substrate adjacent the tunnel junction barrier," a "gate electrode 11 on the second gate insulator and the third gate insulator," and "first and second impurity-doped regions 7, 8 in the substrate coupled by a channel through the first and second portions of the substrate." Office Action, p. 3. This argument reveals a misunderstanding of distinctions between the claimed invention and the structure shown in Song, as the cited structures in Song do not include features corresponding to the recited ***third gate insulator***, the gate electrode ***on the third gate insulator***, and ***a channel through the first and second portions of the substrate*** of Claim 1.

Applicant notes that FIGs. 1(a) of Song shows a tunnel junction barrier transistor having a sidewall gate electrode WORD LINE and a storage node MEMORY NODE on a channel between two impurity-doped regions labeled "SENSE LINE" and "GROUND." Similarly, FIG. 1(d) of Song shows a tunnel junction barrier transistor having a sidewall gate electrode 11 and a storage node 6 on a channel between two impurity-doped regions 7, 8. However, there is no "third gate insulator" or a gate electrode "on the third gate insulator" in either of these figures. In particular, referring to FIG. 1(a) of Song, the doped impurity regions SENSE LINE and GROUND shown in FIG. 1(a) extend all the way to underneath the storage node MEMORY NODE. There is no place for a third insulated gate (*i.e.*, a gate electrode on a gate insulator overlying a channel region in the substrate) adjacent the memory node. The same is true for the structure shown in FIG. 1(d), *i.e.*, the impurity-doped regions 7, 8 extend at least to the edge of the storage node 6, leaving no room for an insulated gate structure adjacent the memory node 6. Therefore, Applicant submits that the cited material from Song does not disclose or suggest, among other things, "***a third gate insulator*** on a second portion of the substrate adjacent the tunnel junction barrier," "a gate electrode on the second gate insulator ***and the third gate insulator***," or "first and second impurity-doped regions in the substrate coupled by ***a channel through the first and second portions of the substrate,***" as recited in Claim 1. For at least these reasons, Applicant submits that Claim 1 is patentable over Song.

Independent Claim 13 recites:

> A memory device, comprising:
> a semiconductor substrate;
> a tunnel junction barrier transistor having a storage node on the substrate, a tunnel junction barrier on the storage node, and a gate electrode on a sidewall of the tunnel junction barrier that controls a channel of the tunnel junction barrier transistor;
> a first planar transistor having a first channel in the substrate disposed transverse to the channel of the tunnel junction barrier transistor and controlled by the storage node of the tunnel junction barrier transistor; and
> ***a second planar transistor having a second channel in the substrate disposed adjacent to the first planar transistor and transverse to the channel of the tunnel junction barrier transistor and having a gate electrode electrically coupled to the gate electrode of the tunnel junction barrier transistor.***

FIGs. 2 and 3 also illustrate embodiments of Claim 13. The region 105a provides "a storage node" and the region 110a provides "a tunnel junction barrier." A vertical portion of the layer 132a on a sidewall of the region 110a provides "a gate electrode" of the tunnel junction barrier transistor. The storage electrode 105a, gate insulator 103a, channel region 140 and adjacent channel/source/drain regions 145a, 145b provide "a first planar transistor." Horizontal portions of the layer 130 and the layer 132a overlying channel/source/drain region 145b provide "a second planar transistor."

Along lines discussed above, the cited material from Song shows structures corresponding to a tunnel junction barrier transistor and a planar transistor having the storage node of the tunnel junction barrier transistor as its gate electrode. However, there is nothing in the cited material that corresponds to the recited "second planar transistor" of Claim 13. Accordingly, Applicant submits that Song does not disclose or suggest all of the recitations of Claim 13 and, for at least these reasons, Applicant submits that Claim 13 is patentable over Song.

The dependent claims are patentable

Applicant submits that dependent Claims 2-12 and 14-18 are patentable at least by virtue of the patentability of the various ones of Claims 1 and 13 from which they depend. Applicant further submits that several of the dependent claims are separately patentable.

Claim 2 recites "wherein the storage node is on a first channel in the first portion of the substrate, and wherein the gate electrode is on a second channel in the second portion of

the substrate that couples the first channel to the first impurity-doped region," while Claim 3 adds "wherein the second channel is configured to serve as a source/drain for the first channel." In rejecting Claims 2 and 3 as anticipated by Song, the Office Action merely restates the claims and cites FIGs. 1 and 2 of Song without any specific indication as to where the recitations of Claims 2 and 3 are shown in these figures. Office Action, pp. 3 and 4. There is no structure shown in the cited portions of Song that corresponds to the recited arrangement of first and second channels in Claim 2, or a second channel that serves as "a source/drain for the first channel" as recited in Claim 3. For at least these reasons, Applicant submits that Claims 2 and 3 are separately patentable over Song.

Claim 4 adds "a fourth gate insulator on a second sidewall of the tunnel junction barrier and a fifth gate insulator on a third portion of the substrate between the tunnel junction barrier and the second impurity-doped region, . . . wherein the gate electrode is disposed on the fourth and fifth gate insulators." Referring to the example embodiment shown in FIGs. 2 and 3, the vertical portion of the layer 130 on the left sidewall of the region 110a provides "a fourth gate insulator," while the adjacent horizontal portion of the layer 130 provides "a fifth gate insulator." As shown, the gate electrode layer 132 extends onto these fourth and fifth insulators. There is nothing in the cited material from Song that corresponds to such features and, for at least these reasons, Applicant submits that Claim 4 is separately patentable over Song. Applicant submits that Claims 5 and 6 are separately patentable over Song for at least similar reasons to those supporting the separate patentability of Claims 2 and 3.

Claim 8 recites "wherein the gate electrode further comprises conductive sidewall spacers interposed between the portions of the second insulation layer on the sidewalls of the tunnel junction barrier and the continuous conductive layer." The Office Action concedes that Song does not disclose the recited sidewall spacers, but alleges that U.S. Patent No. 6,475,857 to Kim et al. (hereinafter "Kim") provides this missing feature. Office Action, p. 8. Respectfully, portions of Kim immediately following the cited section of column 11 clearly indicate that the spacers 43 shown in FIG. 5(b) are formed from an ***insulating*** material and are temporary features used only for masking in ion implantation, *i.e.*, the sidewall spacers 43 are removed before formation of an conformal etch stop layer 51 and an insulating layer 52. *See* Kim, column 11, line 41 through column 12, line 25. Therefore, Kim does not teach or suggest the recited "conductive sidewall spacers interposed between

the portions of the second insulation layer on the sidewalls of the tunnel junction barrier and the continuous conductive layer" as recited in Claim 8. For at least these reasons, Applicant submits that Claim 8 is separately patentable over Song and Kim. Applicant further submits that Claim 10 is separately patentable for at least similar reasons.

Claim 15, which stands rejected as anticipated by Song, recites "wherein the second planar transistor comprises second channels on respective sides of the first channel." As noted above, for example, the regions 145a, 145b may serve as source/drain regions for one transistor, *i.e.*, the first planar transistor, and channel regions for another transistor, *i.e.*, the second planar transistor. No such structure is shown in FIGs. 2 and 3 of Song. For at least these reasons, Applicant submits that Claim 15 is separately patentable.

Claim 16 recites:

> . . . wherein the gate electrodes of the tunnel junction barrier transistor and the second planar transistor comprise a first continuous conductive layer having a first portion on a first sidewall of the tunnel junction barrier and a second portion that extends transverse to the first portion onto a first one of the second channels of the second planar transistor, and a second continuous conductive layer having a first portion on a second sidewall of the tunnel junction barrier opposite the first sidewall and a second portion that extends transverse to the first portion onto a second one of the second channels of the second planar transistor.

An example of such a structure is shown in FIGs. 8 and 9 of the present application, where the regions 221b on respective sides of the structure 214 may be viewed as providing respective recited first and second continuous conductive layers as recited in Claim 16. There is nothing in FIGs. 1 and 2 of Song that discloses or suggests such recitations. In particular, referring to FIGs. 1(a) and (d), the electrodes WORD LINE and 11 do not have "a second portion that extends transverse to the first portion onto a first one of the second channels of the second planar transistor" or "a second portion that extends transverse to the first portion onto a second one of the second channels of the second planar transistor." For at least these reasons, Applicant submit that Claim 16 is separately patentable.

Applicant requests consideration and acknowledgment of Supplemental Information Disclosure Statement submitted June 10, 2005

Applicant notes that the Office Action does not indicate consideration of Applicant's Supplemental Information Disclosure Statement (IDS) submitted June 10, 2005, a copy of which is attached, along with a copy of a return postcard indicating receipt of the IDS in the

U.S. Patent and Trademark Office on June 13, 2005. Applicant respectfully requests consideration of the references cited in the IDS and return of a copy of the initialed form PTO-1449 indicating such consideration.

Conclusion

Applicant submits that the claims are in condition for allowance for at least the reasons discussed above. As all of the claims are now in condition for allowance, Applicant respectfully requests allowance of the claims and passing of the application to issue in due course. Applicant urges the Examiner to contact Applicant's undersigned representative at (919) 854-1400 to resolve any outstanding issues.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 10, 2005.

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